Abstract: This paper provides a technical overview of DisplayPort Ver.1.0, a truly open, pending VESA standard for AV connectivity. DisplayPort is designed to be a scalable and extensible technology foundation for sending digital display and associated data not only between a PC and a display but also between ICs within a system. Its maximum bandwidth is sufficient to support 2560x1600-resolution with pixel bit depth of 30 bits per pixel over a single DisplayPort cable. For inside-the-box application, it reduces the number of wires: LCD panel resolution of up to 1680x1050 can be supported over a single high-speed differential pair. DisplayPort consists of a uni-directional Main Link for transporting isochronous A/V streams from Source device to Sink device and a half-duplex, bi-directional AUX CH used for realizing robust plug-n-play ease of use. Both Main Link and AUX CH are made of AC-coupled differential pairs. The Main Link may have 1, 2, or 4 pairs (or lanes), each capable of supporting application bandwidth of 270Mbytes/second while AUX CH has 1 pair. DisplayPort requires no pair for forwarding clock, thus enabling the maximum usage of the differential pairs. Adopting a layered and modular architecture, DisplayPort can take leverage the advancement of the Physical Layer without affecting upper layers. Based on “micro-packet” architecture, DisplayPort is seamlessly extensible for supporting transport of multiple A/V streams and other data types for new display applications.

Structure of DisplayPort

The DisplayPort link consists of the Main Link, AUX CH, and the Hot Plug Detect (HPD) signal line. As shown in the following diagram, the Main Link is a uni-directional, high-bandwidth, and low-latency channel used for transport of isochronous streams such as uncompressed video and audio. AUX CH is a half-duplex, bi-directional channel used for link management and device control. The HPD signal also serves as an interrupt request by the Sink device.

Main Link

The Main Link consists of AC-coupled, doubly-terminated differential pairs, or lanes. AC-coupling allows the DisplayPort transmitter and receiver to have different common mode voltages. This facilitates the silicon process migration into deep sub-micron (for example, 65 nm CMOS process) while supporting the 0.35 um CMOS process still common for LCD panel TCON (timing controller) chips.

Two link rates are supported: 2.7Gbps and 1.62Gbps per lane. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values M and N. The capabilities of the DisplayPort transmitter and receiver, and the quality of the channel (that is, a cable) will determine whether the link rate is set to 2.7Gbps or 1.62Gbps per lane.

The number of lanes of the Main Link is 1, 2, or 4 lanes. The number of lanes is decoupled from the pixel bit depth (bits per pixel, or bpp) and component bit depth (bits per component, or bpc). Component bit depths of 6, 8, 10, 12, and 16 are supported with the colorimetry formats of RGB, YCbCr444/422 in DisplayPort proposed Version 1.0, regardless of the number of Main Link lanes.

All lanes carry data: there is no dedicated channel for forwarding clock. The link clock is extracted from the data stream itself that is encoded with ANSI8B/10B coding rule (specified in ANSI X3.230-1994, clause 11).

Source and Sink devices are allowed to support the minimum number of lanes required for their needs. The devices that support 2 lanes are required to support both 1 and 2 lanes, while those that support 4 lanes are required to support 1, 2, and 4 lanes. The external cable that is detachable by an end user is required to support 4 lanes for maximizing the interoperability between Source and Sink devices. When fewer than 4 lanes are enabled, those lanes with lower lane numbers (from Lane 0) must be used.

Excluding the 20% channel coding overhead, the DisplayPort Main Link provides for the application bandwidth (also called link symbol rate) of 270Mbytes per second per lane at a high bit rate mode and 162Mbytes per second per lane at a low bit rate mode.

DisplayPort devices may freely trade pixel bit depths with the resolution and frame rate of a stream within the available bandwidth. Examples are shown below.

Over 4 lanes

- 12-bpc YCbCr444 (36 bpp), 1920x1080p @ 96Hz
• 12-bpc YCbCr422 (24 bpp), 1920x1080p @ 120Hz
• 10-bpc RGB (30 bpp), 2560x1536 @ 60Hz

**Over 1 lane**

• 10-bpc YCbCr444 (30 bpp), 1920x1080i @ 60Hz
• 6-bpc RGB (18 bpp), 1680x1050 @ 60Hz

**AUX CH**

AUX CH consists of an AC-coupled, doubly terminated differential pair. Manchester II coding is used as the channel coding for AUX CH. As is the case with the Main Link, clock is extracted from the data stream. The AUX CH transaction starts with the transmission of a synchronization pattern (that is, preamble) to synchronize the sending and receiving devices.

AUX CH is half-duplex, bi-directional. The Source device is the master and the Sink device the slave. As such, all the AUX CH transactions are initiated by the Source device. However, the Sink device may prompt the initiation of an AUX CH transaction by sending an interrupt request (IRQ) to the Source device by toggling the HPD signal. This IRQ feature facilitates the support of Remote Control Command support as specified in CEA-931-B standard.

AUX CH provides for 1Mbps of data rate over the supported cable lengths. Furthermore, each transaction takes no more than 500 us because the maximum burst data size is limited 16 bytes. This way, one AUX CH application starving other applications is avoided.

AUX CH syntax is defined in a way that enables a seamless support of I²C transaction over AUX CH.

**Layered, Modular Architecture**

The diagram below shows the layered architecture of DisplayPort.

![Layered Architecture Diagram](image)

**Figure 2. Layered Architecture**

In the above diagram, DPCD (DisplayPort Configuration Data) in the Sink device describes the capability of the receiver, just as EDID describes that of the Sink device. In addition, DPCD stores the link status information to indicate whether the link is synchronized or not, for link maintenance purpose.

Link and Stream Policy Makers manage the link and the stream, respectively. How they are implemented (state machine, firmware, or system software) is implementation specific. Below Policy Makers and Stream Source/Sink are Link Layer and Physical Layer.

**Link Layer**

Link Layer provides for the following services:

- Isochronous transport services
- Link and Device Services

**Isochronous Transport Services**

Isochronous transport services in the Source device map the video stream and secondary-data packet (for example, audio stream) into the Main Link with a set of rules, so that the streams can be properly reconstructed into the original format and time base by the Sink device. The data-mapping of a stream to the Main Link is devised to facilitate the support of various lane counts.

Following control symbols are used for framing:

- BS (Blank Start), BE (Blank End)
- FS (Fill Start), FE (Fill End)
- SS (Secondary-data Start), SE (Secondary-data End)

The table below shows how the pixel data is steered into the Main Link lanes.

**Table 1. Pixel-steering into Main Link lanes**

<table>
<thead>
<tr>
<th>Number of Lanes</th>
<th>Pixel Steering (N is 0 or positive integer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>Pixel 4N to Lane 0</td>
</tr>
<tr>
<td></td>
<td>Pixel 4N+1 to Lane 1</td>
</tr>
<tr>
<td></td>
<td>Pixel 4N+2 to Lane 2</td>
</tr>
<tr>
<td></td>
<td>Pixel 4N+3 to Lane 3</td>
</tr>
<tr>
<td>2</td>
<td>Pixel 2N to Lane 0</td>
</tr>
<tr>
<td></td>
<td>Pixel 2N+1 to Lane 1</td>
</tr>
<tr>
<td>1</td>
<td>All pixels to Lane 0</td>
</tr>
</tbody>
</table>

This pixel-steering rule applies regardless of the color space/pixel bit depth of the video stream. Since the pixel bit depths supported in DisplayPort Ver.1.0 are larger than 8 bits, each link symbol (which is one byte or 8 bits) carries a part of a pixel data. At the beginning of an active period of the main stream video line, the first partial pixel data symbols immediately follow the BE symbols on all lanes.

The steered pixel data is packed into a Micro-Packet which is called the TU (or Transfer Unit). The TU is 64 symbols long per lane. The length of the TU is fixed to limit the size of buffers needed.
As shown in the diagram below, stuffing symbols are inserted when the DisplayPort transmitter does not have enough valid symbols to transmit within the TU. The FS and FE are the framing symbols indicating the start and end of stuffing symbols, respectively.

![Diagram of stuffing symbols](image)

**Figure 3. Transfer Unit**

The ratio of the valid symbol to stuffing symbol is determined by the ratio between the packed data stream rate and the link symbol rate. Depending on the packed stream rate relative to link symbol rate, a certain number of valid symbols will accumulate every 64 link symbol clock cycles. The DisplayPort transmitter will transmit those valid symbols over the Main Link while the next accumulation starts. This process will repeat until the end of a video line is reached, which is marked by the insertion of BS symbol on all the lanes.

Following the BS symbol, a data symbol called VB-ID is inserted onto all lanes. The following information is conveyed by VB-ID:

- Vertical Blank flag
- Field flag (for interlaced video)
- Interlace flag
- No video flag
- Audio mute flag

DisplayPort does not transmit Hsync and Vsync pulses over the link. Rather, the main-video-stream attribute information necessary for the receiver to regenerate Hsync and Vsync pulses is sent in the Main Stream Attribute packet. Besides horizontal and vertical timing information, colorimetry format information and time stamps for main video stream clock recovery are transmitted in the packet.

Audio and other secondary-data packets may be optionally transported during the horizontal and vertical blanking period of the main video stream.

The highest audio bandwidth expected is about 6Mbytes/sec (= 192kSamples/sec * 32 bits/Sample * 8-ch). Transport of this audio stream is supported over the DisplayPort link for any of the video formats specified in VESA DMT and CVT timing standards and CEA-861-C standard with minimum lane count and link rate necessary to support the given video format.

Data integrity is enhanced for the Main Stream Attribute packet and the optional Secondary-data packet to realize the symbol error rate of 1E-12. For the Main Stream Attribute packet, redundancy including majority voting is used. For the optional Secondary-data packet, Reed-Solomon-based ECC (error correcting code) is used.

**Link and Device Services**

Link Service is used for discovering, configuring, and maintaining the link by accessing DPCD via AUX CH.

Upon hot-plug detection, the Source device reads the capability of the DisplayPort receiver in the Sink device and configures the link through Link Training. The link is enabled with the proper link rate, lane count, and drive current/equalization level, through the handshake between the DisplayPort transmitter and receiver via AUX CH. Link Training is designed to be completed within 10 ms.

After the completion of the Link Training, the DisplayPort transmitter will enter into normal operation. The transmitter keeps the link active by transmitting "Idle Pattern" until there is a stream to transmit. During normal operation, the Sink device may notify the link status change, for example, loss of synchronization, by toggling the HPD signal, thus, sending an interrupt request. The Source device then checks the link status via AUX CH and takes corrective action. This closed-loop link operation enhances the robustness and interoperability between Source and Sink devices.

The Device Service supports device-level applications such as EDID (Extended Display Identification Data) access and MCCS (Monitor Control Command Set) support through AUX CH read/write transactions.

**Physical Layer**

The Physical Layer is divided into two sub-blocks:

- **Logical sub-block**
  - Scrambling/de-scrambling of data (for Main Link)
  - Encoding/Decoding (ANSI8B/10B for Main Link and Manchester II for AUX CH)

- **Electrical sub-block**
  - SERDES (Serialization/Deserialization)
  - Differential current driving/receiving
  - Pre-emphasis/equalization (for Main Link)

The DisplayPort Physical Layer specification realizes BER (bit error rate) equal to or better than 1E-9, even over a 15-meter cable. An extensive amount of channel simulation has been performed to validate that the eye opening requirement at DisplayPort receiver chip pins can be met over the worst-case (though still within the specification) cable-connector assemblies and PCB traces.

The absence of a clock channel and a lower count of active lanes help lower the EMI. In addition, scrambling of data symbols prior to ANSI8B/10B encoding eliminates the
fixed serial bit pattern, thus reducing the EMI when a video stream contains a fixed image (for example, many letter H's scrolling on a screen which is a common test pattern for EMI testing). Furthermore, down-spreading of the link rate (0.5%) is optionally supported for further EMI reduction.

Connectors

The DisplayPort connectors for box-to-box connection are shown below. The 20-pin connector is compact enough that four of them will fit on a PCI-e bracket. It also fits on the back of an ultra-slim notebook PC.

Extensibility

The layered architecture allows DisplayPort to replace the Physical Layer in the future while the Link Layer and above stays intact. Speed upgrade to Generation 2, which will double the per-lane bandwidth, is anticipated a few years after the 1st generation of DisplayPort specification. Connector specifications make a speed upgrade to Gen2 possible without requiring modification to the pin out and form factor.

Furthermore, micro-packet-based transport enables a seamless extension of the DisplayPort specification toward supporting multiple audio-visual streams and other data types. With Gen1 bandwidth, the 4-lane Main Link provides for enough bandwidth to transport six HD (either 1080i or 720p) streams simultaneously. Taking advantage of “micro-packet” architecture, packet overhead may be kept to about 10% or less. Furthermore, less than 1Kbytes of buffer may be required.

Not only the Main Link but also AUX CH is extensible. The AUX CH data rate may be extended enough to support the transport of captured video and voice from Sink device to Source device.

References